REMARKS

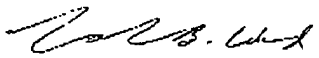
The Examiner objected to the drawings because the Examiner maintains the "integrated circuits elements constructed thereon [first surface of substrate], and extending a maximum distance...into said substrate," and "vias extending...greater than said maximum distance..." are not, according to the Examiner, shown in the drawings. Applicant submits that the claims as amended above are adequately supported in the drawings.

Refering to Figure 1, layer 22 is the circuit layer, layer 21 is the substrate layer, element 51 shows a filled via extending from the top surface of substrate 20 through the circuit layer into layer 21. Since the claim is now written in terms of the via extending into a substrate layer that lacks circuit elements, the details of the circuit elements within the circuit layer are no longer needed to understand the claims. Hence, Applicant is free to show the layers as labeled representations.

Accordingly, Applicant submits that the drawings do not require any corrections, since the circuit layer on top of a substrate layer is clearly shown in the drawings. Furthermore, the claims in question are not defective for lack of support because the claims are supported in the specification.

I hereby certify that this paper is being sent by FAX to 703-872-9306.

Respectfully Submitted,



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